REMARKS

Claims 9-19 are pending in the application.

Claim 19 is rejected under 35 U.S.C. §102(b) as being unpatentable over Mehlhorn et al. (U.S. Pat. No. 6,285,808).

Claims 9-18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Mehlhorn et al. and further in view of Su (U.S. Pat. No. 6,787,919).

Claim 16 is rejected under 35 U.S.C. §103(a) as being unpatentable over Mehlhorn et al. and Su and further in view of Yoshimura et al (U.S. Pat. No. 6,706,546).

Claim 9 has been amended to more clearly define the subject matter applicants regard as patentable over the cited prior art references. More specifically, the multiplexer, the demultiplexer, the optical filter, the micro-electrical-mechanical system and the optical amplifier of the electrically controlled optical add-drop multiplexer are integrated within at least one optical layer of a multilayer printed circuit board. The multilayer printed circuit board comprising various components recited in amended claim 9 including an optical waveguide formed within the at least one optical layer whereby the optical waveguide carries the optical signal to the electrically controlled optical add-drop multiplexer. Applicants respectfully submit that amended claim 9 and all claims depending there from are allowable over Mehlhorn et al. and Su.

Mehlhorn et al. teaches that surface-mounted electro-optical components can be fixed in the usual way to circuit carries, such as soldering the component to a circuit board, and that an optical connection with an optical layer may be made at the same time. This allows for dispensing with the conventional connections with optical fibers, for example, at the surface of the circuit board. The device of Mehlhorn et al. includes an optical layer 1 that is surrounded by a circuit board layer 2 and a circuit board layer 3. An electro-optical component 4 is attached to the surface of circuit board layer 2 so that an optical connection 6 of the component faces toward an optical deflecting system 9, which may direct an optical signal into the optical layer 1.

Su teaches an opto-electronic circuit, such as a thermo-optic switch (TOS) 105, coupled to a package substrate through solder bumps 232, which provide electrical connections to the opto-electronic circuit. An exemplary embodiment of Su teaches that the TOS 105, which is

formed on a substrate 100, is coupled to a package substrate 150 at conductive strips 151, 152 and 153 via solder bump technology. Package substrate 150 may include conductive pads 161, 162 and 163 so that it may be connected with a circuit board using solder bumps. These pads may also assist with heat dissipation from the TOS 105.

FIG. 2 of Su illustrates a generic opto-electronic device 200 attached to a circuit board 220. Device 200 is coupled with a package substrate 210 via solder bump technology comprising conductive pads 230, solder bumps 232 and conductive strips 234. Package substrate 210 may have multiple layers, which allows for interconnects 250 to be formed within the package substrate 210. This allows for more flexibility in designing the layouts of conductive pads 230 and conductive strips 234, and may also assist with heat dissipation. The teachings of Su are limited to opto-electronic devices 200, such as TOS 105, that are solder bumped to a package substrate 210 then ultimately solder bumped to a circuit board 220.

Applicants respectfully submit that neither Mehlhorn et al. nor Su teach, disclose or otherwise suggest the invention as delineated in amended claim 9. Further, neither Mehlhorn et al. nor Su provide any motivation to one skilled in the art to combine their respective teachings in such a way to arrive at the invention as defined in amended claim 9. The essence of Mehlhorn et al. teaches to surface-mount an electro-optical device on a circuit board in order to eliminate conventional connections with optical fibers at the surface of the circuit board. This allows for reliable operation and makes simple and automated fabrication possible. The essence of Su teaches to different approaches for connecting a packaged opto-electronic device onto a circuit board by using solder bump technology.

The Examiner cites column 1, lines 64-65 of Mehlhorn et al. as teaching applying the invention to a plurality of electro-optical components, and column 1, lines 12-21 of Su as disclosing a variety of optical circuits including opto-electronic integration devices. The cited portion of Mehlhorn et al. discloses very generally that surface-mountable electro-optical components can be fixed in the usual way to circuit boards, typically by soldering. The cited portion of Su refers to the generally functionality of optical circuits and that planar lightwave circuits (PLC) are optical circuits that are manufactured and operate in the plane of the circuit. PLC technology may be used to form small-scale components and their structures may be batch fabricated on a silicon wafer. However, applicant respectfully submits that neither of these references teaches, suggests or provides incentive to one skilled in the art to form an electrically

controlled optical add-drop multiplexer within an optical layer of a multilayer printed circuit board as defined in amended claim 9 and claims depending there from.

Claim 16 has also been amended herein to more clearly define the subject matter claimed as patentable over the cited prior art. More specifically, a plurality of optical conductor paths are formed within the multilayer printed circuit board that have three-dimensional optical structures such that two optical conductor paths arranged in different layers of the multilayer printed circuit board are optically connected to one another. In view of the above, applicants respectfully submit that amended claim 16 is in condition for allowance.

Claim 19 has been canceled.

In view of the foregoing amendment and remarks, applicants respectfully request entry of this amendment and reconsideration of the application.

Conclusion

The commissioner is hereby authorized to charge any appropriate fees due in connection with this paper, including the fees specified in 37 C.F.R. §§ 1.16 (c), 1.17(a)(1) and 1.20(d), or credit any overpayments to Deposit Account No. 19-2179.

Respectfully submitted,

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